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10/666,317	09/19/2003	David Mui	8377/ETCH/SILICON/JB	7907

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EXAMINER	
CHEN, ERIC BRICE	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,317	MUI ET AL.	
	Examiner	Art Unit	
	Eric B. Chen	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/19/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) *24-28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-28* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-23, drawn to a method, classified in class 438, subclass 706.

   II. Claims 24-28, drawn to a computer-readable medium, classified in class 711, subclass 4.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I and II are related as method and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the method as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case, the method can be performed without the using a computer-readable medium containing instructional software.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. Furthermore, because the search required for Invention I is not required for Invention II, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with Keith P. Taboada on May 11, 2005 a provisional election was made without traverse to prosecute Invention I, claims 1-23. Affirmation of this election must be made by applicant in replying to this Office action.

Claims 24-28 withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Priority

6. Applicant is advised of possible benefits under 35 U.S.C. 119(a)-(d), wherein an application for patent filed in the United States may be entitled to the benefit of the filing date of a prior application filed in a foreign country.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. *See In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

8. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

9. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1 and 7-10 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-9, 11, and 13-14 of copending Application No. 10/690,318, Mui et al., filed Oct. 21, 2003 (U.S. Patent Appl. Pub. No. 2005/0085090). This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

11. As to claim 1, Mui claims a method for controlling dimensions of structures formed on a substrate using an etch process (Preliminary Amendment, filed Sept. 20, 2004, claim 8, page 8, lines 4-5), comprising: providing the substrate having a patterned etch mask formed thereon (claim 8, page 8, lines 6-7); measuring dimensions of elements of the mask on the substrate (claim 8, page 8, lines 8-9); adjusting a process recipe for an etch process using the results of measuring said dimensions (claim 8, page 8, lines 15-16); and forming the structures on the substrate performing the etch process that uses the adjusted process recipe (claim 8, page 8, line 12). Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicants' claim 1 is generic to all that is recited in claim 8 of Mui

in Application No. 10/690,318. That is, claim 8 of Mui falls entirely within the scope of Applicants' claim 1 or, in other words, Applicants' claim 1 is anticipated by claim 8 of Mui. Specifically, Mui's claim 8 contains additional limitations, such as trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed (claim 8, page 8, lines 10-11), which are not claimed by the Applicant.

12. As to claim 7, Mui claims that the measuring technique is an optical measuring technique (claim 9, page 8, lines 18-19).

13. As to claim 8, Mui claims that the measuring step and the forming step are performed using processing modules of a single substrate processing system (claim 11, page 8, lines 24-25).

14. As to claim 9, Mui claims that the adjusting step comprises calculating an adjustment for the process recipe of the etch process (claim 13, page 8, line 31; page 9, line 1).

15. As to claim 10, Mui claims the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the structures during the etch process (claim 14, page 9, lines 3-5).

16. Claims 12 and 19-23 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 16-17, 19, 21, and 23-27 of copending Application No. 10/690,318, Mui et al., filed Oct. 21, 2003.

17. As to claim 12, Mui claims a method for controlling dimensions a gate structure of a field effect transistor formed on a substrate using an etch process, comprising (claim 16, page 9, lines 9-10): providing the substrate having a patterned etch mask formed upon a film stack of the gate structure (claim 16, page 9, lines 11-12); measuring dimensions of elements of the mask on the substrate (claim 16, page 9, lines 13-14); adjusting a process recipe for an etch process of etching a layer of the film stack using the results of measuring said dimensions (claim 16, page 9, lines 20-21); and forming the structures in the layer performing the etch process that uses the adjusted process recipe (claim 16, page 9, line 17). Although the conflicting claims are not identical, they are not patentably distinct from each other because Applicants' claim 12 is generic to all that is recited in claim 16 of Mui in Application No. 10/690,318. That is, claim 16 of Mui falls entirely within the scope of Applicants' claim 12 or, in other words, Applicants' claim 12 is anticipated by claim 16 of Mui. Specifically, Mui's claim 16 contains additional limitations, such as trimming the patterned mask on the at least one substrate using a process recipe based on the measurements performed (claim 16, page 9, lines 15-16), which are not claimed by the Applicant.

18. As to claim 19, Mui claims that the measuring technique is an optical measuring technique (claim 17, page 9, lines 23-24).

19. As to claim 20, Mui claims that the measuring step and the forming step are performed using processing modules of a single substrate processing system (claim 19, page 9, lines 29-30).

20. As to claim 21, Mui claims that the adjusting step comprises calculating an adjustment for the process recipe of the etch process for etching the layer (claim 21, page 10, lines 6-8; claim 23, page 10, lines 13-15).

21. As to claim 22, Mui claims that the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the layer during the etch process (claim 24, page 10, lines 17-20).

22. As to claim 23, Mui claims that the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases (claim 26, page 10, lines 25-27), a plasma source power, a substrate bias power (claim 27, page 10, lines 29-30; page 11, lines 1-6), a material of the structures and a thickness of sidewalls of the structures (claim 24, page 10, lines 17-20; claim 25, page 10, lines 22-23).

Claim Rejections - 35 USC § 102

23. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

24. Claims 1-13, 15, and 17-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Tao et al. (U.S. Patent No. 6,620,631).

25. As to claim 1, Tao discloses a method for controlling dimensions of structures formed on a substrate using an etch process, comprising: providing the substrate (10) (column 6, lines 37-41) having a patterned etch mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed thereon (Figure 1); measuring dimensions of elements of the mask (14a/14b/14c/14d/14e) on the substrate (10) (column 8, lines 50-61); adjusting a process recipe for an etch process using the results of measuring said dimensions (column 9, lines 11-15); and forming the structures on the substrate performing the etch process that uses the adjusted process recipe (column 10, lines 42-51; Figure 2).

26. As to claim 2, Tao discloses that the substrate (10) is a semiconductor wafer (column 6, lines 37-41).

27. As to claim 3, Tao discloses that the mask (14) is a patterned hard etch mask or a patterned photoresist mask (column 7, lines 35-47).

28. As to claim 4, Tao discloses that the structures are formed in at least one material layer (12) disposed beneath the mask (column 6, lines 33-36; Figures 1-2).

29. As to claim 5, Tao discloses that the dimensions are smallest widths of the elements (column 5, lines 15-20).

30. As to claim 6, Tao discloses that the dimensions are measured using a non-destructive measuring technique (column 8, lines 50-61).

31. As to claim 7, Tao discloses that the measuring technique is an optical measuring technique (column 8, lines 50-61).

32. As to claim 8, Tao discloses that the measuring step and the forming step are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

33. As to claim 9, Tao discloses that the adjusting step comprises calculating an adjustment for the process recipe of the etch process (column 9, lines 11-15).

34. As to claim 10, Tao discloses that the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the structures during the etch process (column 9, lines 20-32).

35. As to claim 11, Tao discloses that the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures (column 9, lines 20-37).

36. As to claim 12, Tao discloses a method for controlling dimensions a gate structure of a field effect transistor (column 5, lines 56-63) formed on a substrate using an etch process, comprising: providing the substrate (10) (column 6, lines 37-41) having a patterned etch mask (14a/14b/14c/14d/14e) (column 7, lines 35-37) formed upon a film stack of the gate structure (12) (column 7, lines 21-31; Figure 1); measuring dimensions of elements of the mask (14a/14b/14c/14d/14e) on the substrate (10) (column 8, lines 50-61); adjusting a process recipe for an etch process of etching a layer of the film stack using the results of measuring said dimensions (column 9, lines

11-15); and forming the structures in the layer performing the etch process that uses the adjusted process recipe (column 10, lines 42-51; Figure 2).

37. As to claim 13, Tao discloses that the layer (12) is selected from a group consisting of a gate conductor layer and a gate electrode layer (column 7, lines 21-31).

38. As to claim 15, Tao discloses that the mask (14) is a patterned hard etch mask or a patterned photoresist mask (column 7, lines 35-47).

39. As to claim 17, Tao discloses that the dimensions are smallest widths of the elements (column 5, lines 15-20).

40. As to claim 18, Tao discloses that the dimensions are measured using a non-destructive measuring technique (column 8, lines 50-61).

41. As to claim 19, Tao discloses that the measuring technique is an optical measuring technique (column 8, lines 50-61).

42. As to claim 20, Tao discloses that the measuring step and the forming step are performed using processing modules of a single substrate processing system (column 5, lines 38-44).

43. As to claim 21, Tao discloses that the adjusting step comprises calculating an adjustment for the process recipe of the etch process for etching the layer (column 9, lines 11-15).

44. As to claim 22, Tao discloses that the adjustment is an adjustment for at least one parameter related to a thickness of a film of the material removed from sidewalls of the layer during the etch process (column 9, lines 20-32).

45. As to claim 23, Tao discloses that the at least one parameter is selected from a group consisting of a duration of time for overetching the structures, a flow rate and/or pressure of an etchant gas or gases, a plasma source power, a substrate bias power, a material of the structures and a thickness of sidewalls of the structures (column 9, lines 20-37).

Claim Rejections - 35 USC § 103

46. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

47. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tao in view of Wolf, *Silicon Processing for the VLSI Era*, Vols. 1 and 4, Lattice Press (1986, 2002) and Streetman, *Solid State Electronic Devices*, Prentice Hall (1990).

48. As to claim 14, Tao discloses that the gate electrode layer comprises doped polysilicon (column 7, lines 23-25).

49. Tao does not expressly disclose that the gate conductor layer comprises WSi. However, Wolf teaches for field effect transistor devices, delays in interconnect switching can be reduced by incorporating low resistivity materials (vol. 1, page 384). Moreover, refractory silicides, such as WSi_2, $TiSi_2$, $MoSi_2$, $TaSi_2$, are used as a gate electrode material (vol. 1, page 385). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate conductor

layer of WSi. One who is skilled in the art would be motivated to incorporate WSi to reduce the delays in interconnect switching.

50. Tao does not expressly disclose that the gate dielectric layer comprises SiO_2 or HfO_2. However, Tao's method is directed at patterning gate electrodes for field effect transistors (column 5, lines 56-63). Streetman teaches that in forming conventional field effect transistors, a SiO_2 gate dielectric layer is formed below the gate electrode ("G" in Figure 8-8(a), page 300). Wolf teaches a need for high-k dielectrics ($k > 7$) in metal-oxide-semiconductor field effect transistors, due to the increase in undesirable tunneling effects associated with thinner gate oxides, a result of device miniaturization (vol. 4, page 145). Wolf teaches that many important high-k materials are currently under investigation as a replacement for silicon oxide as a gate dielectric, including HfO_2 (vol. 4, page 145-46). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the gate dielectric layer of SiO_2 or HfO_2. One who is skilled in the art would be motivated to form a conventional structure with SiO_2, because such a structure has been successfully implemented as an operational semiconductor device. Furthermore, one who is skilled in the art would be motivated to find a high-k material replacement for silicon oxide, such as HfO_2, as a gate dielectric to reduce the undesirable tunneling effects.

51. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tao in view of Wolf and Streetman, in further view of Zhou et al. (U.S. Patent No. 5,858,847).

52. As to claim 16, Tao does not expressly disclose that the mask comprises a material selected from a group consisting of SiON, SiO_2, Si_3N_4, HfO_2 and α-carbon. Tao

discloses that the hard masking material may be formed of those conventional in the art (column 7, lines 35-47). Zhou teaches that in forming a field effect transistor (column 1, lines 37-43), hard mask (22) is formed over the field oxide region (12) (column 3, lines 8-10). Hard mask (22) is used as both an etch barrier to etch the gate electrode (19) and as a mask to form the source and drain regions by ion implantation (column 3, lines 20-25). Moreover, Zhou teaches that hard mask (22) can be formed of silicon oxide, silicon nitride or silicon oxynitride (column 4, lines 40-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the mask of a material selected from a group consisting of SiON, SiO_2, Si_3N_4, HfO_2 and α-carbon. One who is skilled in the art would be motivated to select a conventional hard mask material that can also be used as an ion implantation mask.

Conclusion

53. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Stirton (U.S. Patent No. 6,479,200) discloses a method of controlling photoresist exposure by scatterometric techniques. Bonser et al. (U.S. Patent No. 6,245,581) discloses a method for controlling the critical dimensions of a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric B. Chen whose telephone number is (571) 272-

2947. The examiner can normally be reached on Monday through Friday, 8AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine G. Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EBC EBC
May 19, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER